

REMARKS

Claims 1, 4-7, 10-13, 15, 18, 21-23, and 25-27 are pending.
Claims 1, 7, 15, and 18 are in independent form.

Rejections under 35 U.S.C. § 101

In the action mailed July 13, 2007, claims 1 and 15 were rejected under 35 U.S.C. § 101 as allegedly being directed to nonstatutory subject matter. As best understood, the rejection contends that a processor must be functionally coupled to a module that is potentially made out of software for a system that includes the module to produce a tangible result. See, e.g., Office action mailed July 13, 2007, page 3, para. 4.9.3; page 5, para. 4.19.3.

Although applicant disagrees, to advance prosecution, claims 1 and 15 have been amended to recite logic design modules that are operable on one or more data processing devices. Further, claim 15 has been amended to recite modification logic that is operable on one or more data processing devices.

Accordingly, applicant respectfully requests that the rejections of claims 1 and 15 be withdrawn.

Objections to the Claims

Claim 1 was objected to as failing to require a functionally connected processing element. As discussed above, claim 1 has been amended to recite a logic design module that is operable on one or more data processing devices. Accordingly, Applicant respectfully requests that the objection to claim 1 be withdrawn.

Rejections under 35 U.S.C. § 112

Claim 15 was rejected under 35 U.S.C. § 112 as indefinite. Although applicant disagrees with the rejection, as discussed above, claim 15 has been amended to recite a logic design module that is operable on one or more data processing devices and modification logic that is operable on one or more data processing devices. Accordingly, Applicant respectfully requests that the objection to claim 15 be withdrawn.

Rejections under 35 U.S.C. § 103

Claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,226,776 to Panchul (hereinafter "Panchul") and the publication entitled "A Multi-Representational Design Data Capture System," by K. Yamagishi (hereinafter "Yamagishi"), and the publication entitled "IEEE

Standard Hardware Description Language Based on the Verilog® Hardware Description Language" (hereinafter "IEEE Std. 1364-1995").

As amended, claim 1 relates to a system that includes a logic design module operable on one or more data processing devices to be used by one or more users to generate a logic design as part of an electrical circuit and a central database integrated with the logic design module and including a collection of modifiable values of signal parameters that are accessible by the logic design module. The logic design includes labels. The values of signal parameters are associated with the labels in the logic design. The logic design module is operable to update the logic design to reflect modification of the values of the signal parameters in the central database by modifying the logic design to be compatible with the modified values of the signal parameters, and to indicate design discrepancies in the logic design resulting from the modifications to the values of the signal parameters in the central database automatically. The collection of modifiable values is separate from the logic design.

The rejection contends that it would have been obvious for one of ordinary skill to combine Panchul, Yamagishi, and the IEEE Std. 1364-1995 to arrive at the subject matter recited in claim 1.

Applicant respectfully disagrees. In this regard, Panchul describes a system for converting a high-level language program to a hardware design implementation. *See, e.g., Panchul*, col. 4, line 3-8. A user initially renders a preliminary hardware design in a standard high-level programming language. *See, e.g., Panchul*, col. 12, line 34-37. *See also Panchul*, col. 12, line 51-67. Panchul's system then compiles the high-level programming language into a hardware description language (HDL) synthesizable design. *See, e.g., Panchul*, col. 13, line 33-37. The HDL design is then synthesized into a gate-level hardware representation. *See, e.g., Panchul*, col. 13, line 53-57. *See also Panchul*, col. 12, line 42-45. In turn, the gate-level hardware representation can be reduced to an actual hardware implementation. *See, e.g., Panchul*, col. 13, line 64-col. 14, line 16; col. 12, line 45-47.

Panchul neither describes nor suggests that a collection of modifiable values separate from the logic design are associated with labels in either Panchul's preliminary hardware designs or HDL designs. In this regard, as discussed above, Panchul's preliminary hardware designs are in a standard high-level programming language. *See also Panchul*, col. 14, line 16-35. There is no description or suggestion in Panchul that a collection of modifiable values that are associated with labels in Panchul's preliminary hardware designs is separate from the

preliminary hardware designs. Instead, Panchul's preliminary hardware designs are understood to be self-contained in standard high-level programming language.

Moreover, there is no description or suggestion in Panchul that such labels are somehow inserted into a logic design when the preliminary hardware designs are compiled into an HDL design or that a collection of modifiable values is somehow created. Indeed, FIGS. 3-27 of Panchul show numerous examples of the compilation of high-level C-type programs into HDL representations. *See, e.g., Panchul*, col. 8, line 5-col. 11, line 37. None of these are understood to describe or suggest that labels are inserted into the hardware designs represented preliminarily in the standard high-level programming languages, or that a separate collection of modifiable values of signal parameters that are associated with such labels is somehow created.

The rejection is understood to point to the definitions of ADDRESS_SIZE and DATA_SIZE in Panchul's FIG. 18B1 as allegedly showing such labels. Applicant respectfully disagrees. In standard high-level programming languages, such as illustrated in Panchul's FIG. 18B1, such definitions are part of the code. In Panchul, this code is the preliminary hardware design. The

ADDRESS_SIZE and DATA_SIZE definitions thus do not label the preliminary hardware design and are not separate from the preliminary hardware design.

Further, since Panchul's system compiles such a unlabeled high-level programming language into an HDL design, Applicant understands the HDL designs formed by such compiling to also be unlabeled. Accordingly, Panchul's HDL designs also do not describe or suggest that a logic design include labels or that a collection of modifiable values separate from Panchul's HDL designs are associated with such labels.

Finally, Panchul's synthesis of the HDL design into a gate-level hardware representation and reduction of the gate-level hardware representation into an actual hardware implementation are "conventional" and "do not constitute [Panchul's] invention per se." *See, e.g., Panchul*, col. 12, line 45-47; col. 13, line 53-57; col. 13, line 60-61. Applicant also submits that nothing in Panchul's synthesis and reduction of gate-level hardware representations describes or suggests that a logic design include labels or that a separate collection of modifiable values are associated with such labels.

Yamagishi and the IEEE Std. 1364-1995 do not remedy these deficiencies in Panchul. Indeed, Yamagishi at least suggests that an exhaustive array of different design data be maintained in a single "design entity." *See, e.g., Yamagishi*, § 2.1.

Accordingly, nothing in Yamagishi would lead one of ordinary skill to modify Panchul so that a collection of modifiable values separate from a logic design are associated with labels in a logic design, as recited in claim 1.

As for the cited portion of the IEEE Std. 1364-1995, this portion deals with specifying a range of repetitive instances. These specifications are understood to be part of the code that constitutes a hardware design. Accordingly, nothing in IEEE Std. 1364-1995 would lead one of ordinary skill to modify Panchul so that a collection of modifiable values separate from a logic design are associated with labels in the logic design, as recited in claim 1.

Thus, even if Panchul, Yamagishi, and the IEEE Std. 1364-1995 were combined, one of ordinary skill would not arrive at a collection of modifiable values of signal parameters that is separate from the logic design and that are accessible by a logic design module to update the logic design to reflect modification thereof. Accordingly, claim 1 is not obvious over Panchul, Yamagishi, and the IEEE Std. 1364-1995. Applicant respectfully requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

Claim 7 was rejected under 35 U.S.C. § 103(a) as obvious over Panchul, Yamagishi, and IEEE Std. 1364-1995.

As amended, claim 7 relates to a computer-implemented method that includes receiving an assignment of a value to a signal parameter, maintaining the value of the signal parameter in a central database in association with an identifier of the signal parameter, using the identifier of the signal parameter maintained in the central database to identify a first position in computer code for a logic design forming part of an electrical circuit, modifying the computer code at the first position to reflect the value, using the identifier of the signal parameter maintained in the central database to identify a second position in the computer code for the logic design, modifying the computer code at the second position to reflect the value, receiving an updated value of the signal parameter in the central database, updating both the first position and the second position in the computer code for the logic design to reflect the updated value of the signal parameter, and indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically. The value of the signal parameter is maintained separately from the computer code for the logic design.

Panchul, Yamagishi, and IEEE Std. 1364-1995 neither describe nor suggest modifying computer code for a logic design at first and second positions to reflect the value of a signal parameter maintained separately from the computer code for the logic design in a central database, as recited in claim 7.

In this regard, as discussed above, Panchul's preliminary hardware designs are understood to be self-contained in standard high-level programming language. Panchul's HDL designs and gate-level hardware representations are produced from the self-contained preliminary hardware designs and also believed to be self-contained.

Thus, Panchul neither describes nor suggests modifying computer code for a logic design at first and second positions to reflect the value of a signal parameter maintained separately from the computer code for the logic design in a central database, as recited in claim 7.

Yamagishi and the IEEE Std. 1364-1995 do not remedy these deficiencies in Panchul. Indeed, Yamagishi at least suggests that an exhaustive array of different design data be maintained in a single "design entity," while the cited portion of IEEE Std. 1364-1995 deals with specifications of ranges of repetitive instances in the code that constitutes a hardware design. Accordingly, nothing in Yamagishi and the IEEE Std. 1364-1995 would lead one of ordinary skill to modify computer code for a

logic design at first and second positions to reflect the value of a signal parameter maintained separately from the computer code for the logic design in a central database, as recited in claim 7.

Thus, even if Panchul, Yamagishi, and the IEEE Std. 1364-1995 were combined, one of ordinary skill would not arrive at the recited subject matter. Accordingly, claim 7 is not obvious over Panchul, Yamagishi, and the IEEE Std. 1364-1995. Applicant respectfully requests that the rejections of claim 7 and the claims dependent therefrom be withdrawn.

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Panchul and Yamagishi, and IEEE Std. 1364-1995.

As amended, claim 15 relates to an apparatus that includes a central database accessible by one or more users, modification logic operable on one or more data processing devices to allow a user to modify the values associated with identifiers individually, and an interface to convey the identifiers and the associated values from the central database to a logic design module that is operable on one or more data processing devices and that uses the identifiers to identify where a logic design is to be changed and the values to change a bit width in the logic design to form part of an electrical circuit. The central database includes a collection of identifiers of one or more bit width signal parameters and values associated with each of the

identifiers of the bit width signal parameters. The collection of identifiers of one or more bit width signal parameters is maintained separately from the logic design.

Panchul and Yamagishi neither describe nor suggest a central database that includes a collection of identifiers of one or more bit width signal parameters and values associated with each of the identifiers, wherein the collection of identifiers is maintained separately from a logic design, as recited in claim 15.

In this regard, as discussed above, Panchul's preliminary hardware designs are understood to be self-contained in standard high-level programming language. Panchul's HDL designs and gate-level hardware representations are produced from the self-contained preliminary hardware designs and also believed to be self-contained.

Thus, Panchul neither describes nor suggests a collection of identifiers of one or more bit width signal parameters and values associated with each of the identifiers, wherein the collection of identifiers is maintained separately from a logic design, as recited in claim 15.

Yamagishi does not remedy these deficiencies in Panchul. Indeed, Yamagishi at least suggests that an exhaustive array of different design data be maintained in a single "design entity." Accordingly, nothing in Yamagishi would lead one of ordinary

skill to a collection of identifiers of one or more bit width signal parameters and values associated with each of the identifiers, wherein the collection of identifiers is maintained separately from a logic design, as recited in claim 15.

Thus, even if Panchul and Yamagishi were combined, one of ordinary skill would not arrive at the recited subject matter. Accordingly, claim 15 is not obvious over Panchul and Yamagishi. Applicant respectfully requests that the rejections of claim 15 and the claims dependent therefrom be withdrawn.

Claim 18 was rejected under 35 U.S.C. § 103(a) as obvious over Panchul, Yamagishi, and IEEE Std. 1364-1995.

As amended, claim 18 relates to a machine-accessible medium containing instructions which cause a machine to perform operations. The operations include receiving a value of a signal parameter that characterizes multiple bits of a multiple bit signal, maintaining the value of the signal parameter in a central database, using the value of the signal parameter that is maintained in the central database in computer code for a logic design forming part of an electrical circuit that includes the multiple bit signal, receiving an update to the value of the signal parameter in the central database, updating the logic design with the updated value of the signal parameter by modifying the logic design to be compatible with the updated value of the signal parameter, and indicating design

discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically. The value of the signal parameter is maintained separately from the computer code for the logic design.

Panchul, Yamagishi, and IEEE Std. 1364-1995 neither describe nor suggest modifying a logic design to be compatible with an updated value of the signal parameter, where the value of the signal parameter is maintained separately from the computer code for the logic design, as recited in claim 18.

In this regard, as discussed above, Panchul's preliminary hardware designs are understood to be self-contained in standard high-level programming language. Panchul's HDL designs and gate-level hardware representations are produced from the self-contained preliminary hardware designs and also believed to be self-contained.

Thus, Panchul neither describes nor suggests modifying a logic design to be compatible with an updated value of the signal parameter, where the value of the signal parameter is maintained separately from the computer code for the logic design, as recited in claim 18.

Yamagishi and the IEEE Std. 1364-1995 do not remedy these deficiencies in Panchul. Indeed, Yamagishi at least suggests that an exhaustive array of different design data be maintained in a single "design entity," while the cited portion of IEEE

Std. 1364-1995 deals with specifications of ranges of repetitive instances in the code that constitutes a hardware design.

Accordingly, nothing in Yamagishi and the IEEE Std. 1364-1995 would lead one of ordinary skill to modify a logic design to be compatible with an updated value of the signal parameter, where the value of the signal parameter is maintained separately from the computer code for the logic design, as recited in claim 18.

Thus, even if Panchul, Yamagishi, and the IEEE Std. 1364-1995 were combined, one of ordinary skill would not arrive at the recited subject matter. Accordingly, claim 18 is not obvious over Panchul, Yamagishi, and the IEEE Std. 1364-1995. Applicant respectfully requests that the rejections of claim 18 and the claims dependent therefrom be withdrawn.

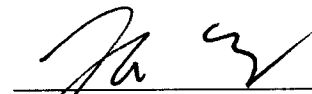
It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as

specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant asks that all claims be allowed. Please apply the one-month extension of time fee and any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: November 13, 2007



John F. Conroy
Reg. No. 45,485

Fish & Richardson P.C.
PTO Customer No. 20985
12390 El Camino Real
San Diego, California 92130
(858) 678-5070 telephone
(858) 678-5099 facsimile

JFC/jhg
10784592.doc